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EXAMINER	
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ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,001	ZHANG ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Notice

1. In view of the Appeal Brief filed on 9th of October 2006 (hereinafter the Appeal Brief), PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
10/30/06

Receipt Acknowledgement

2. Receipt is acknowledged of the Amendment After Final filed on 11th of May 2006. Claims 1, 9, 19, and 24 have been amended; no claim has been canceled; and no claim has been newly added since the Final Office Action was mailed on 15th of March 2006. The after final amendment that was not entered before is entered and considered on the merits (See M.P.E.P. 1207.04[R-3]). Currently, claims 1-24 are pending in this Application.

Claim Objections

3. Claim 24 is objected to because of the following informalities:

It recites the subject matter "the ensuing bus grants" in lines 2-3, and the subject matter "the ensuing bus grant indications" in line 4. However, they have not been specifically clarified in the claim 24, and its intervening claims. Therefore, the Examiner presumes that the terms "the ensuing bus grants" and "the ensuing bus grant indications" could be considered as --the grant indications-- in light of the claimed invention since it is not clearly defined in the claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. [US 5,526,508 A; hereinafter Park].

Referring to claim 1, AAPA discloses a method for transferring information to a bus (i.e., Bus 106 of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising:

- receiving an indication (i.e., CPU_WR_COM or CPU_RD_COM) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to a bus (i.e., Bus 106 of Fig. 1; See page 8, paragraph [0028]);
- reading a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]);
- writing the information (i.e., said CAD, CDW, and CCO) to a buffer (i.e., Two-Entry Buffer 202 of Fig. 2); and
- transferring the information (i.e., said information CAD, CDW, and CCO in said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information to the bus is allowed (See page 9, paragraph [0029]).

AAPA does not teach said writing the information to said buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed; and bypassing the buffer and said transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed.

Park discloses a method for cache line replacing system (See Fig. 3 and Abstract), wherein said method (i.e., said method for cache line replacing system) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) including

- writing an information (i.e., line of cache data) to a buffer (i.e., RD Buffer 36 of Fig. 3) if a bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 5, in other words, said CPU/Cache bus is occupied by said write back cycle; See col. 6, lines 11-14); and
- bypassing the buffer (See Title; bypassing said RD buffer) and
- transferring the information (i.e., said line of cache data) to the bus (i.e., said CPU/Cache bus) if the buffer (i.e., said RD Buffer) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is allowed for memory read cycle after write back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, for the advantage of providing a way that a device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

Referring to claim 2, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes

- a write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 9, paragraph [0030], lines 11-13),
- an address (i.e., CPU_ADDR on CAD in Fig. 3; See page 9, paragraph [0030], lines 6-9), and
- data to be written to the address (i.e., CPU_DATA_WR on CDW in Fig. 3; See page 9, paragraph [0030], lines 9-10).

Referring to claim 3, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
  - the write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 8, paragraph [0028], lines 6-9).

Referring to claim 4, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
  - a read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 11, paragraph [0036], lines 8-10) and
  - an address from which data is to be read (i.e., CPU_ADDR on CAD in Fig. 4; See page 11, paragraph [0036], lines 5-8).

Referring to claim 5, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
    - the read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 8, paragraph [0028], lines 9-11).

Referring to claim 6, AAPA teaches

- access to the bus (i.e., Bus 106 of Fig. 1) is controlled by a bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) employing a bus parking protocol (i.e., bus parking scheme; See PARKING_GNT in Figs. 3-4, and page 9, paragraph [0029]).

Referring to claim 7, AAPA teaches

- sending a bus access request (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) if the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) does not indicate that transfer of the information to the bus is allowed (i.e., Bus 106 of Fig. 1 is not available; See page 7, paragraph [0025], lines 10-13, page 9, paragraph [0029], and page 17, paragraph [0048], lines 4-11).

Referring to claim 8, AAPA teaches

- periodically sending bus access requests (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) and reading the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) if the information stored in the buffer has not been transferred to the bus (See page 15, paragraph [0045], line 1 through paragraph [0046], line 12), so that when the bus grant indication indicates that transfer of the information to the bus allowed (i.e., bus

is available), the information stored in the buffer is transferred to the bus (See page 2, paragraph [0004], lines 5-8).

Referring to claim 9, AAPA discloses a bus interface unit (i.e., conventional BIU 105 in Fig. 1; See page 7, paragraph [0023], lines 1-4) in information transfers from a device (i.e., CPU 101 of Fig. 1) to a bus (i.e., Bus 106 of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising:

- a buffer (i.e., Two-Entry Buffer 202 of Fig. 2) having inputs coupled to the device (i.e., said CPU; See Figs. 1-2, and page 7, paragraph [0025], lines 1-3) and
- logic (i.e., Control Logic 201 of Fig. 2) configured to
  - receive an indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., said CPU) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., said Bus; See page 8, paragraph [0028]),
  - read a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]), and
  - cause the information (i.e., said CAD, CDW, and CCO) to be stored in the buffer (i.e., said Two-Entry Buffer), and to be transferred from the buffer (i.e., said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information from the buffer to the bus is allowed (See page 9, paragraph [0029]).

AAPA does not teach said logic being configured to cause the information to either be stored in the buffer if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus, thereby

bypassing the buffer, if the buffer is empty and the transfer of the information to the bus is allowed.

Park discloses a cache line replacement apparatus (See Fig. 3 and Abstract), wherein a bus interface unit (i.e., said cache line replacement apparatus) for reducing latency in information transfers (See col. 3, lines 2-3) from a device (i.e., Main Memory 100 of Fig. 3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) including

- logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) configured to
    - cause an information (i.e., line of cache data) to either be stored in a buffer (i.e., RD Buffer 36 of Fig. 3) if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed (i.e., said CPU/Cache bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 5, in other words, said CPU/Cache bus is occupied by said write back cycle; See col. 6, lines 11-14), or be transferred from the device (i.e., said Main Memory) to the bus (i.e., said CPU/Cache bus), thereby bypassing the buffer (See Title; bypassing said RD buffer); if the buffer (i.e., said RD Buffer) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is allowed for memory read cycle after write back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said logic (i.e., MUX and Buffer WT Reg), as disclosed by Park, in said logic (i.e., Control Logic), as disclosed by AAPA, for the advantage of providing a way that said device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

Referring to claim 10, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
    - a write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 9, paragraph [0030], lines 11-13),
    - an address (i.e., CPU_ADDR on CAD in Fig. 3; See page 9, paragraph [0030], lines 6-9), and
    - data to be written to the address (i.e., CPU_DATA_WR on CDW in Fig. 3; See page 9, paragraph [0030], lines 9-10).

Referring to claim 11, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
    - the write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 8, paragraph [0028], lines 6-9).

Referring to claim 12, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
    - a read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 11, paragraph [0036], lines 8-10) and
    - an address from which data is to be read (i.e., CPU_ADDR on CAD in Fig. 4; See page 11, paragraph [0036], lines 5-8).

Referring to claim 13, AAPA teaches

- the indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., CPU 101 of Fig. 1) that information (i.e., CAD, CDW, and CCO in Figs. 2-3) is to be transferred to the bus (i.e., Bus 106 of Fig. 1) includes
    - the read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 8, paragraph [0028], lines 9-11).

Referring to claim 14, AAPA teaches

- access to the bus (i.e., Bus 106 of Fig. 1) is controlled by a bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) employing a bus parking protocol (i.e., bus parking scheme; See PARKING_GNT in Figs. 3-4, and page 9, paragraph [0029]).

Referring to claim 15, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to send a bus access request (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) if the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) does not indicate that transfer of the information to the bus is allowed (i.e., Bus 106 of Fig. 1 is not available; See page 7, paragraph [0025], lines 10-13, page 9, paragraph [0029], and page 17, paragraph [0048], lines 4-11).

Referring to claim 16, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to periodically send bus access requests (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) and read the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) if the information

stored in the buffer has not been transferred to the bus (See page 15, paragraph [0045], line 1 through paragraph [0046], line 12), so that when the bus grant indication indicates that transfer of the information to the bus allowed (i.e., bus is available), the logic (i.e., said Control Logic) causes the information stored in the buffer is transferred to the bus (See page 2, paragraph [0004], lines 5-8).

Referring to claim 17, AAPA, as modified by Park, teaches

- the logic (i.e., Control Logic 201 in Fig. 2; AAPA, MUX 38 and Buffer WT Reg 37 in Fig. 3; Park) includes
    - a multiplexer (i.e., MUX 38 of Fig. 3; See Park, col. 4, lines 40-46) having
        - first inputs (i.e., input of said MUX being coupled to Memory Bus 32 in Fig. 3; Park) coupled to the buffer inputs (i.e., RD Buffer 36 being coupled to said Memory Bus 32 in Fig. 3; Park),
        - second inputs (i.e., input of said MUX being coupled to Bus Line 33 in Fig. 3; Park) coupled to the buffer outputs (i.e., output of said RD Buffer; Park),
        - outputs coupled to the bus (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3; Park), and
        - at least one select input (i.e., input from said Buffer WT Reg 37 in Fig. 3; Park) for selectively coupling either the first or the second inputs to the outputs (See Park, col. 3, lines 27-35); and
- the logic (i.e., said Control Logic of AAPA, and said MUX/Buffer WT Reg of Park) is further configured to provide

- a control output (i.e., output of said Buffer WT Reg) to the at least one select input (See Park, Fig. 3) so that the first inputs (i.e., input of said MUX being coupled to said Memory Bus of Park) are coupled to the outputs (i.e., output of said MUX being coupled to said CPU/Cache Bus of Park) if the bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See AAPA, page 9, paragraph [0029]) indicates that transfer of the information to the bus is allowed (See AAPA, page 9, paragraph [0029], and see Park, col. 3, lines 27-35, and col. 4, lines 31-46, i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer) and the buffer (i.e., RD Buffer 36 of Fig. 3; Park) is empty (i.e., said Buffer WT Reg counts 'zero'; See Park, col. 5, lines 26-30).

Referring to claim 18, Park teaches

- the logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) is further configured to provide
  - the control output (i.e., output of said Buffer WT Reg) to the at least one select input (See Fig. 3) so that the second inputs (i.e., input of MUX being coupled to Bus Line 33 in Fig. 3) are coupled to the outputs (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3) if the bus grant indication does not indicate that transfer of the information to the bus (i.e., said CPU/Cache Bus) is allowed (i.e., said CPU/Cache Bus is not busy due to write-back buffering during a cache line replacing cycle, which is clearly implies the bus grant indication does not indicate that transfer of the information to the bus is allowed; See col. 4, lines 31-36).

Referring to claim 19, AAPA discloses in a computer system (i.e., in a conventional Computer System 100 in Fig. 1) including

- a bus (i.e., Bus 106 of Fig. 1) with access governed by a bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) employing a bus parking scheme (See PARKING_GNT in Figs: 3-4, and page 9, paragraph [0029]) and
- a buffer (i.e., Two-Entry Buffer 202 of Fig. 2) having inputs coupled to a device (i.e., CPU 101 of Fig. 1) so that
    - information (i.e., CAD, CDW, and CCO in Figs. 2-3) to be transferred from the device to the bus is stored in the buffer (See page 7, paragraph [0025]).

AAPA does not teach said information to be transferred from the device to the bus is stored in the buffer if a bus grant indication generated by the bus arbiter indicates that the bus is unavailable for the transfer, or the bus grant indication indicates that the bus is available for transfer of the information to the bus, and a buffer bypass circuit for reducing latency in information transfers to the bus comprising: a multiplexer having first inputs coupled to inputs to the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

Park discloses a cache line replacement apparatus (See Fig. 3 and Abstract), wherein information (i.e., line of cache data) to be transferred from device (i.e., Main Memory 100 of Fig. 3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) is stored in a buffer (i.e., RD Buffer 36 of Fig. 3) if a bus grant indication generated by a bus arbiter (i.e., means for controlling cache line replacing cycles; See Abstract) indicates that the bus is unavailable for the transfer (i.e., said CPU/Cache

bus is not allowed to be used by memory read cycle during write back cycle of the steps 51 and 52 in Fig. 5, in other words, said CPU/Cache bus is occupied by said write back cycle; See col. 6, lines 11-14), or the bus grant indication indicates that the bus is available for transfer of the information to the bus (i.e., said CPU/Cache bus is allowed for memory read cycle after write back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46), and a buffer bypass circuit (i.e., said cache line replacement apparatus) for reducing latency in information transfers (See col. 3, lines 2-3) to the bus (i.e., said CPU/Cache bus) comprising:

- a multiplexer (i.e., MUX 38 of Fig. 3; See col. 4, lines 40-46) having
  - first inputs (i.e., input of said MUX being coupled to Memory Bus 32 in Fig. 3) coupled to inputs to the buffer (i.e., said RD Buffer being coupled to said Memory Bus in Fig. 3),
  - second inputs (i.e., input of said MUX being coupled to Bus Line 33 in Fig. 3) coupled to outputs of the buffer (i.e., output of said RD Buffer),
  - outputs coupled to the bus (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3), and
  - at least one select input (i.e., input from Buffer WT Reg 37 in Fig. 3) for selectively coupling either the first or the second inputs to the outputs (See col. 3, lines 27-35); and
- logic (i.e., MUX 38 and Buffer WT Reg 37 in Fig. 3) configured to provide
  - control information (i.e., MUX control information from said Buffer WT Reg) to the at least one select input (i.e., input of said MUX being coupled to said Memory Bus) such that the first inputs (i.e., input of said MUX being coupled to said Memory Bus) are coupled to the outputs of the multiplexer (i.e., output of said MUX being coupled

to said CPU/Cache Bus) if the buffer (i.e., said RD Buffer) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and the bus is available for transfer of the information to the bus (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said buffer bypass circuit, as disclosed by Park, in said logic (i.e., Control Logic), as disclosed by AAPA, for the advantage of providing a way that said device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

Referring to claim 20, AAPA, as modified by Park, teaches

- the logic (i.e., Control Logic 201 in Fig. 2; AAPA, MUX 38 and Buffer WT Reg 37 in Fig. 3; Park) is further configured to provide
  - control information (i.e., MUX control information from said Buffer WT Reg; Park) to the at least one select input (i.e., input of said MUX being coupled to said Memory Bus; Park) generated such that after checking the bus grant indication (i.e., checking GNT/PARKING-GNT in Fig. 2; See AAPA, page 9, paragraph [0029]) the second inputs (i.e., input of MUX being coupled to Bus Line 33 in Fig. 3; Park) are coupled to the outputs of the multiplexer (i.e., output of said MUX being coupled to CPU/Cache Bus 31 in Fig. 3; Park) if the buffer (i.e., RD Buffer 36 of Fig. 3; Park) is not empty (See Park, col. 3, lines 27-32 and col. 4, lines 40-44) and the bus grant indication indicates that the bus is available for transfer of the information to the bus (See AAPA, page 9, paragraph [0029], lines 9-13), or the bus grant indication does not

indicate that the bus is available for transfer of the information to the bus (i.e., when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO; AAPA, and Park suggests the input of MUX being coupled to said Bus Line is still connected to the outputs of the multiplexer as long as the count value of said Buffer WT Reg is larger than zero; See Park, col. 4, lines 42-44).

Referring to claim 21, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
  - a write command (i.e., CPU_WR_COM on CCO in Fig. 3; See page 9, paragraph [0030], lines 11-13),
  - an address (i.e., CPU_ADDR on CAD in Fig. 3; See page 9, paragraph [0030], lines 6-9), and
  - data to be written to the address (i.e., CPU_DATA_WR on CDW in Fig. 3; See page 9, paragraph [0030], lines 9-10).

Referring to claim 22, AAPA teaches

- the information (i.e., CAD, CDW, and CCO in Figs. 2-3) includes
  - a read command (i.e., CPU_RD_COM on CCO in Fig. 4; See page 11, paragraph [0036], lines 8-10) and
  - an address from which data is to be read (i.e., CPU_ADDR on CAD in Fig. 4; See page 11, paragraph [0036], lines 5-8).

Referring to claim 23, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to send a bus access request (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) if the bus grant indication (i.e., GNT/PARKING-GNT in Fig. 2) does not indicate that the bus is available for transfer of the information to the bus (i.e., Bus 106 of Fig. 1 is not available; See page 7, paragraph [0025], lines 10-13, page 9, paragraph [0029], and page 17, paragraph [0048], lines 4-11).

Referring to claim 24, AAPA teaches

- the logic (i.e., Control Logic 201 of Fig. 2) is further configured to periodically send bus access requests (i.e., REQ in Fig. 2) to the bus arbiter (i.e., Bus Arbiter 107 of Fig. 1) and read the bus grant indications (i.e., GNT/PARKING-GNT in Fig. 2) if the information stored in the buffer has not been transferred to the bus (See page 15, paragraph [0045], line 1 through paragraph [0046], line 12), so that when one of the bus grant indications indicates that the bus is available for transfer of the information to the bus (i.e., bus is allowed to transfer), the information stored in the buffer is transferred to the bus (See page 2, paragraph [0004], lines 5-8).

Response to Arguments

7. Applicants' arguments in the Appeal Brief filed on 9th of October 2006 with respect to all the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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CEL/